REMARKS

Claims 1-16 are presently pending. Claims 1-13 were rejected. Claims 14-16 are added. Reconsideration and continued examination are respectfully requested in view of the foregoing amendments and following remarks.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Rana and Agarwal. Final Office Action at 2. Claim 1 recites, among other limitations, "the contents of the memory location associated with the address received from the code address bus being incremented responsive to receipt of the address".

Examiner has indicated that "Rana does not teach the contents of the memory location associated with the address received form the code address bus being incremented responsive to the receipt of the address, however, Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" to determine if the code has been executed (See Col. 8, lines 31-44). Agarwal discloses code coverage testing and flagging code that has been executed. In addition to just flagging the code that has been executed, Agarwal also teaches incrementing a value of the associated memory (see Agarwal, pargraphs 0123, 0124, and 0127)." FOA at 3.

Examiner further notes that "The rejection has not be[en] written to replace the flag of Rana with the incremented value of Agarwal, but rather combin[e] the two together, therefore still retaining the full functionality of the flag of Rana and further including the incremented value of Rana."

As an initial matter, it is respectfully noted that

Examiner indicated that Rana teaches "storing code coverage data of predetermined bit patterns" and that Agarwal teaches "flagging code that has been executed" and "incrementing a value of the associated memory".

To the extent that Examiner, indeed, maintains the rejection of claim 1, over "retaining the full functionality of the flag of Rana and further including the incremented value of Rana", Assignee respectfully traverses because even Examiner has indicated that "Rana does not teach the contents of the memory location associated with the address received form the code address bus being incremented responsive to the receipt of the address".

Rather, it is believed that when Examiner indicated "combined the two together, retaining the full functionality of the flag of Rana and further including the incremented value of Rana", Examiner intended to refer to "predetermined bit patterns" of Rana and the "incremented value" of Agarwal.

However, Assignee respectfully traverses the rejection of claim 1. If "Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" to determine if the code has been executed", the "code coverage memory" could not include "the incremented value" of Agarwal, in combination, because "the incremented value" of Agarwal would overwrite the "predetermined bit patterns" of Rana, thereby rendering Rana unsatisfactory for its intended purpose.

Accordingly, Assignee respectfully traverses the rejection to claims 1, 5, and 9, as well as to dependent claims 2-4, 6-8, and 10-13.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being

obvious from the combination of Rana and Agarwal. Claim 2 recites, among other limitations, "an address multiplexer for making a first selection between the input and an address counter, and for providing the first selection to the memory". Examiner has indicated that Rana and Agarwal disclose "the code coverage memory being concurrently addressed with the monitored memory and use of counter circuit of memory location is isolated from the addressing from the monitored memory, thus selecting counter circuit and the address lines being multiplexed, this is interpreted as an address multiplexer for making a selection between the input and an address counter and for providing the selection to the memory".

Assignee respectfully traverses and submits that even if "counter circuit of memory location is isolated from the addressing from the monitored memory, thus selecting counter circuit", the foregoing does not teach "an address multiplexer for making a first selection between the input and an address counter, because the "counter circuit" would always be selected. Accordingly, Assignee respectfully traverses the rejection to claim 2, and claim 10.

Moreover, further in regards to claim 10, that recites, among other limitations, "an address multiplexer connected to the input and address counter", Assignee respectfully traverses the rejection because even if "the code coverage memory being concurrently addressed with the monitored memory and use of counter circuit of memory location is isolated from the addressing from the monitored memory, thus selecting counter circuit and the address lines being multiplexed", there is no teaching that the "address multiplexer" is "connected to the input". Accordingly, Assignee traverses the rejection to claim 10.

Additionally, newly added claim 14 recites, among other limitations, "a first input that is directly connected to the input for receiving an address from a code address bus; a second input that is directly connected to the address counter; and an output that is directly connected to the memory." Assignee respectfully submits that even if "the code coverage memory being concurrently addressed with the monitored memory and use of counter circuit of memory location is isolated from the addressing from the monitored memory, thus selecting counter circuit and the address lines being multiplexed", claim 14 is allowable, at least because there is no teaching that the "address multiplexer" comprises "a first input that is directly connected to the input for providing connected to the input for receiving and address from a code address bus".

Newly added claim 15 recites, among other limitations, "wherein multiplexer directly connects the first input to the output if the input for receiving an address from a code address bus is the first selection and directly connects the second input to the output if the address counter is the first selection". Although Examiner indicates that the combination of Rana and Agarwal disclose "selecting counter circuit", because "the cover[age] memory is isolated from addressing [the] monitored memory", the foregoing does not teach "wherein multiplexer directly connects the first input to the output if the input for receiving an address from a code address bus is the first selection". Accordingly, for at least the foregoing reason, claim 15 is allowable.

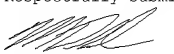
Newly added claim 16 recites, among other limitations, "wherein the first selection is sometimes the input for receiving an address from a code address bus and is sometimes the address counter". Even if "counter circuit of memory location is isolated from the addressing from the monitored memory, thus selecting counter circuit", the foregoing does not teach "wherein the first selection is sometimes the input for receiving an address from a code address bus", because the "counter circuit" would always be selected.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: February 14, 2008

Respectfully submitted,



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